

# APPLICATION UNDER UNITED STATES PATENT LAWS

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(M#)

Invention: METHOD OF FORMING DAMASCENE PATTERN IN A SEMICONDUCTOR DEVICE

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This is a:

- Provisional Application
- Regular Utility Application
- Continuing Application
  - The contents of the parent are incorporated by reference
- PCT National Phase Application
- Design Application
- Reissue Application
- Plant Application
- Substitute Specification  
Sub. Spec Filed \_\_\_\_\_  
in App. No. \_\_\_\_\_ / \_\_\_\_\_
- Marked up Specification re  
Sub. Spec. filed \_\_\_\_\_  
In App. No \_\_\_\_\_ / \_\_\_\_\_

## SPECIFICATION

**METHOD OF FORMING DAMASCENE PATTERN IN A SEMICONDUCTOR  
DEVICE**

**BACKGROUND OF THE INVENTION**

**(a) Field of the Invention**

5       The present invention relates to a method of forming damascene pattern in a semiconductor device, and particularly to a method of forming damascene pattern, which is able to minimize the change of critical dimension of a damascene mask according to the via/contact density.

**(b) Description of Related Art**

10     Recently, copper (Cu) wiring process is suggested to improve characteristics of a semiconductor device such as operation speed, resistance, parasitic capacitance between metal layers, while semiconductor devices become integrated and the fabrication technique is advanced. For insulating films, material having low-k (dielectric constant) is highlighted instead of the conventional oxide films for the 15 wiring process of the next generation device.

However, the wiring process using copper and material having low-k has a disadvantage that etching characteristic of copper is very poor. In this regard, a method of forming damascene pattern in which via holes and trenches are formed by via etching and trench etching and filled with copper as disclosed in US patent No. 20 5,635,423 is known as proper for copper wiring.

However, the conventional method of forming damascene pattern has problems listed below:

One of the methods of forming damascene pattern is shown in Figs. 1 and 2. To form a damascene pattern, as shown in Figs. 1 and 2, a bottom wiring 10 is formed

on a semiconductor substrate (not shown), a thick oxide layer 20 is deposited thereon, via holes 25 are formed in the oxide layer 20 using via etching, a bottom anti-reflection layer 30 is deposited on the surfaces of the oxide layer 20 and the via holes 25, and trenches (not shown) are formed using a mask pattern 40 for trench etching.

5 According to the above method of forming damascene pattern, the bottom anti-reflection layer 30 in the area A1 placed on the left side of Fig.1, i.e. the area with low via hole density is deposited to become thicker than that in the other area A2 placed on the right side of Fig.1, i.e. the area with high via hole density.

That is, the thickness T of the bottom anti-reflection layer 30 deposited on the  
10 area A1 with low via hole density exceeds the thickness T' on the area A2 with high via hole density.

In case that the thickness T and T' of the bottom anti-reflection layer 30 are different ( $T \neq T'$ ), width of a mask pattern 40 for trench etching in the area A1 with low via hole density becomes very different from that in the area A2 with high via hole density ( $W \ll W'$ ) when the mask pattern 40 for trench etching is formed.  
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Therefore, the critical dimension CD of the damascene pattern 50 in the area A1 with low via hole density becomes very different from that in the area A2 with high via hole density ( $CD \ll CD'$ ) due to the difference of the width of the mask pattern 40 for trench etching depending on via hole density as described above. In result,  
20 reliability of the device becomes low due to the low CD uniformity.

#### SUMMARY OF THE INVENTION

An aspect of the present invention is to provide a method of forming damascene pattern in a semiconductor device which is able to minimize the change of

critical dimension of a damascene pattern by minimizing the change of thickness of a bottom anti-reflection layer depending on the via hole density.

According to an embodiment of the present invention, a method of forming damascene pattern in a semiconductor device, which includes forming an insulating layer on a bottom wiring, forming via holes exposing a part of the bottom wiring by removing the insulating layer selectively, filling insides of the via holes to a prescribed thickness, forming an anti-reflection layer on the via holes and the insulating layer, forming a mask pattern for trench etching on the insulating layer on which the anti-reflection layer is formed, and forming a damascene pattern using the mask pattern for trench etching, is provided.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view for describing shortcomings of a conventional method of forming damascene pattern in a semiconductor device;

Fig. 2 is a sectional view showing a damascene pattern formed by the conventional method of forming damascene pattern in a semiconductor device;

Figs. 3-6 are sectional views illustrating process steps of a method of forming damascene pattern in a semiconductor device according to the present invention; and

Fig. 7 is a sectional view of a damascene pattern formed by the method of forming damascene pattern in a semiconductor device of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

Figs. 3-6 are sectional views illustrating process steps of a method of forming damascene pattern in a semiconductor device according to the present invention. In Figs. 3-6, an area A1 placed on the left side is the area with low via hole density, and an area A2 placed on the right side is the area with high via hole density.

5 According to a method of forming damascene pattern in a semiconductor device according to an embodiment of the present invention, as shown in Fig. 3, an insulating layer 200 is formed by depositing an insulating material such as oxide on a bottom wiring 100 made of copper.

10 Next, a mask (not shown) having a prescribed form for via etching is formed on the insulating layer 200, and the insulating layer 200 is removed selectively using the mask. Then, as shown in Fig. 4, via holes 250 exposing a part of the bottom wiring 100 are formed in the insulating layer 200.

Subsequently, as shown in Fig. 5, insides of the via holes 250 are filled with a non-conductive material 280, preferably photoresist or oxide, to a prescribed thickness.

15 It will be described in more detail. First, a non-conductive material layer 280 is formed on the insulating layer 200 in which the via holes are formed. Next, the non-conductive material layer 280 is partly removed by entire surface dry etching or chemical-mechanical polishing (CMP) process to make the insulating layer 200 become exposed and to remain the non-conductive material layer 280 to a prescribed thickness 20 insides the via holes 250.

Succeedingly, a bottom anti-reflection layer 300 which serves as a barrier to prevent the sidewalls of the via holes 250 and the bottom wiring 100 from getting damaged during etching process for forming trench is formed on the via holes 250 and the insulating layer 200.

Since the insides of the via holes 250 are filled with the non-conductive material 280 such as photoresist, thickness T of the bottom anti-reflection layer 300 in the area A1 with low via hole density has substantially no difference from the thickness T' in the area A2 with high via hole density ( $T \approx T'$ ).

5 Next, as shown in Fig. 6, a mask pattern 400 for trench etching is formed on the insulating layer 200 on which the bottom anti-reflection layer 300 is formed.

According to the above-described method, since the thickness of the bottom anti-reflection layer 300 in the area A1 with low via hole density approximates the thickness of the bottom anti-reflection layer 300 in the area A2 with high via hole density ( $T \approx T'$ ), widths W and W' of the mask pattern 400 in the areas A1 and A2 become very close ( $W \approx W'$ ).

Therefore, as shown in Fig. 7, critical dimension CD of the damascene pattern in the area A1 with low via hole density and critical dimension CD' in the area A2 with high via hole density have close values ( $CD \approx CD'$ ).

15 As described in the above, the method of forming damascene pattern in a semiconductor device according to the present invention has an advantage that CD uniformity is improved by minimizing the change of the critical dimension of the damascene pattern, thereby increasing reliability of the semiconductor device.

While the present invention has been described in detail with reference to the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.